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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,855	DA DALT, NICOLA	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

The arguments filed 12/03/2009 that Ng does not disclose "at least two" as required in the amended claims were fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of the teachings of other references already of record.

The arguments (pg 11-12) that Ng does "define any type of lattice arrangement, as defined by the Applicant's claims" are not convincing. The claims do not recite structural limitations that exclude the structure of Ng. The metal layers of Ng are made of materials (e.g., col 4 ln 25-32) known to be at least polycrystalline, each crystal constituting a "lattice", as this term is commonly used in this art.

Claim Rejections - 35 USC § 102

Statute 35 U.S.C. § 102 is the basis for anticipation rejections made herein:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Ng.

RE claim 16, Ng discloses a semiconductor component having an integrated capacitance structure (50; col 6 ln 52-53), capacitance structure comprising (Figs 2-4):

an insulating layer (58, 62, 66; col 6 ln 62&65, col 7 ln 2);

a first metal lattice (68) in the insulating layer including intersecting metal leads (edges 69 at corners; col 7 ln 4-9) in a first common plane and defining a checkerboard

pattern (a rectangle is "a checkerboard pattern" per MPEP § 2111, since such patterns may be seen in a checkerboard, which is essentially colored graph paper);

a second metal lattice (64) in the insulating layer including intersecting metal leads (edges 65 at corners; col 7 ln 4-9) in a second common plane and defining a checkerboard pattern (per MPEP § 2111);

electrically conductive regions (75; col 7 ln 22-24) electrically isolated from the crossing metal leads (75 isolated by dielectric from 68 & 69; Fig 3) and arranged in openings in at least one of the first and second metal lattices, the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer and electrically isolated from one another by the intersecting metal leads,

wherein the intersecting metal leads have a width (width of 69; MPEP § 2111) less than or equal to the distance between the edge regions of the openings and the electrically conductive regions; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice (uppermost 75) are substantially vertically above crossing points of the second metal lattice (64 at 65), and crossing points of the first metal lattice (68 at 69) are substantially vertically above the electrically conductive regions of the second metal lattice (75);

a third metal structure (60; col 8 ln 60) in the insulating layer in a third common plane the third metal structure comprising one of a third metal lattice or a metal plate; and

first and second electrical connections between the first and second lattices such that the first and second electrical connections are at different electrical potential (inherent in connection to different polarities: col 7 ln 21-24, col 8 ln 39-46).

RE claim 17, Ng discloses the third metal structure comprises a metal plate (60) electrically coupled to the electrically conductive regions (75) of the first and second metal lattices by the first and second electrical connections (72, 74; col 7 ln 21-24).

RE claim 18, Ng discloses the third metal structure comprises a third metal lattice including intersecting metal leads (main portion 60 crosses edge 61; col 7 ln 4-9), wherein the intersecting metal leads define openings (either side of 75), wherein the openings are devoid of electrically conductive regions, and wherein the intersecting metal leads are electrically connected to the electrically conductive regions of the first and second metal lattices by the first and second electrical connections (col 7 ln 21-24).

RE claim 19, Ng discloses the first electrical connection (74 on right in Fig 3) electrically connect the electrically conductive regions of the first metal lattice (75) to the crossing points of the second metal lattice (64 at 65), and

wherein the second electrical connection (74 on left in Fig 3) electrically connect the crossing points of the first metal lattice (68 at 69) to the electrically conductive regions of the second metal lattice (75).

RE claim 20, Ng discloses the third metal structure comprises a third metal lattice including intersecting metal leads (60 crosses 61) and electrically conductive regions (75) in openings defined by the intersecting metal leads.

RE claim 21, Ng discloses non-parasitic capacitances exist between the electrically conductive regions and intersecting metal leads in the first, second, and third metal lattices and wherein non-parasitic capacitances exist between the first and second connecting lines (inherent in structure - see MPEP § 2112.01).

Claim Rejections - 35 USC § 103

Statute 35 U.S.C. § 103(a) is the basis for obviousness rejections made herein:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. § 103(a) as unpatentable in view of Ng (US 5,583,359), Kuroda (US 6,370,010) and Baker (US 6,410,955).

RE claim 1, Ng discloses a semiconductor component comprising (Figs 2-4):

a semiconductor substrate (52; col 7 ln 44-46) having an insulating layer (58, 62, 66; col 6 ln 62&65, col 7 ln 2) on the semiconductor substrate surface and having a capacitance structure (50; col 6 ln 52-53) in the insulating layer, wherein the capacitance structure comprises:

a first substructure (top metal layer; 68+75+69 in Fig 1) having a first cohesive latticed metal region including crossing metal leads (edges 69 at corners; col 7 ln 4-9),

the first substructure extending in a first common plane parallel to the substrate surface such that the first substructure has common top and bottom surfaces which limit the first cohesive latticed metal region from above and from below,

wherein the first cohesive latticed metal region is electrically connected to a first connecting line (col 7 ln 21-24, col 8 ln 39-46); and

an electrically conductive region (75; col 7 ln 22-24) in the first substructure and electrically isolated from the crossing metal leads (75 isolated from 68 & 69; Fig 3) and arranged in openings in the first cohesive latticed metal region at a distance from edge regions of the openings in the first common plane,

wherein the crossing metal leads have a width (of 69) equal to the distance between the edge regions of the openings and the electrically conductive region, and

wherein the electrically conductive region is electrically connected to a second connecting line (col 7 ln 21-24, col 8 ln 39-46), and

wherein the electrically conductive region comprises metal plates (75) between via (74; col 7 ln 21) connections electrically isolated from one another by the latticed metal region (e.g., 75 of two adjacent levels).

Ng differs from the claimed invention in not showing at least two electrically conductive regions in the first substructure.

Ng is directed to a multi-layer capacitor for high-frequency circuits (col 1 ln 8-10).

Kuroda is analogously directed to a multi-layer capacitor for high-frequency circuits (col 1 ln 13-15) and teaches a structure having advantageously improved electrical properties (col 3 ln 25-30) stemming from the pattern of current flow within the multi-layer capacitor (col 12 ln 58-62). The particular current patterns (col 8 ln 32-34) are due to alternating and offset (col 7 ln 1-11) first (10, Fig 3A) and second (11, Fig 3B) substructures which each include at least two electrically conductive regions (17 in Fig

3A, 16 in Fig 3B, col 8 ln 3) isolated in cutouts (18, col 8 ln 11-14)) of their respective substructures (col 7 ln 62 – col 8 ln 18).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the capacitor structure of Kuroda in the semiconductor component of Ng, essentially replacing Ng Fig 2 with Kuroda Fig 2, such that the first substructure of Ng then includes at least two electrically conductive regions; at least for a semiconductor component having a capacitor with advantageous electrical properties.

The combination of Ng and Kuroda arguably differs from the claimed invention only in not explicitly disclosing the crossing metal leads having width less than or equal to the distance between the edge regions of the openings.

Ng clearly shows the claimed width relationship, Kuroda seems to depict leads so wide that their crossing essentially defines a sheet with what is depicted as relatively small holes. However, the scope of Kuroda is in no way limited by the width of the leads or the opening size. It seems the designer may choose to adjust the width.

Baker is analogously directed to a capacitor in an integrated circuit (col 1 ln 5-8) and is evidence that the claimed relationship between conductor width (col 4 ln 50) and the distance between edge regions in openings therebetween (col 4 ln 51-52) is known to be a variable affecting the resultant capacitance (col 4 ln 59-64).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in the combined structure of Ng and Kuroda, the crossing metal leads have a width less than or equal to the distance between the edge regions of the openings and the electrically conductive region; at least for the desired capacitance.

RE claim 2, the combination includes, as Kuroda discloses (Figs 3-4), a second substructure (11) parallel to and at a distance from the first substructure (10) wherein the second substructure comprises (Fig 3B):

a second cohesive latticed metal region including crossing metal leads which extend in a second common plane parallel to the substrate surface such that it has common top and bottom surfaces which limit the second latticed metal region from above and below; and

electrically conductive regions (16),

wherein the first and second substructures are electrically connected by the first and second connecting lines (16 & 17, Fig 4, col 7 ln 62 – col 8 ln 18).

RE claim 3, the combination includes, as Kuroda discloses (Figs 3-4), the second substructure is of substantially the same design as the first substructure, and the first and second substructures are laterally offset from one another (col 7 ln 5-8) such that the at least two electrically conductive regions (17) of the first substructure (10) are substantially vertically aligned above crossing points (17) of the metal leads in the second cohesive latticed metal region of the second substructure (11), and crossing points (16) of the metal leads in the first cohesive latticed metal region of the first substructure (10) are substantially vertically aligned above the electrically conductive regions (16) of the second substructure (11).

RE claim 4, the combination includes, as Kuroda discloses (Figs 3-4), the crossing points (16) of the metal leads in the first cohesive latticed metal region of the first substructure (10) are electrically connected to the at least two electrically

conductive regions (16) of the second substructure (11) and the electrically conductive regions (17) of the first substructure (10) are electrically connected to the crossing points (17) of the metal leads in the second cohesive latticed metal region of the second substructure (11) by means of at least one respective via connection (Fig 4, col 7 ln 52).

RE claim 5, the combination includes, as Kuroda discloses (Figs 3-4), the second cohesive latticed metal region of the second substructure (11) is laterally offset (col 7 ln 5-8) from the first substructure (10), so that the at least two electrically conductive regions (17) of the first substructure (105) are substantially vertically aligned above the crossing points (17) of the metal leads in the second cohesive latticed metal region of the second substructure (11).

RE claim 6, the combination includes, as Kuroda discloses, the at least two electrically conductive regions (17) of the first substructure (10) and the crossing points (17) of the metal leads in the second cohesive latticed metal region of the second substructure (11) are electrically connected by means of one or more respective via connections (17, col 7 ln 57).

RE claim 7, the combination includes, as Kuroda discloses (Figs 3-4), a metal plate (14) electrically connected to one of the crossing points (16) of the metal leads in a the cohesive latticed metal region of the first substructure (10) and to the electrically conductive regions (16) of the second substructure (75) by means of one or more respective via connections (72, 74).

RE claim 8, the combination includes, as Kuroda discloses (Fig 3A) the first cohesive latticed metal region has at least two square or round openings (18).

RE claim 9 the combination includes, as Kuroda discloses, the first (16) and second (17) connecting lines are at different electrical potentials (inherently the cause of the current shown, e.g., col 7 ln 32-35, col 8 ln 32-34).

RE claim 10, the combination includes, as Kuroda discloses a first non-parasitic capacitance exists between the crossing metal leads of the cohesive latticed metal region and the at least two electrically conductive regions of the first substructure and a second non-parasitic capacitance exists between the first and second connecting lines, and wherein the magnitude of the first non-parasitic capacitance differs from the magnitude of the second non-parasitic capacitance (inherent; see MPEP § 2112.01).

RE claim 11, Ng discloses a semiconductor component having an integrated capacitance structure, the component comprising (Figs 2-4):

a semiconductor substrate (52; col 7 ln 44-46) having a surface;

an insulating layer (58, 62, 66; col 6 ln 62&65, col 7 ln 2) overlying the surface of the semiconductor substrate;

a capacitance structure (50; col 6 ln 52-53) in the insulating layer, wherein the capacitance structure comprises:

a first metal lattice including intersecting metal leads (edges 69 at corners; col 7 ln 4-9) in a first common plane parallel to the substrate surface;

a second metal lattice including intersecting metal leads (edges 65 at corners; col 7 ln 4-9) in a second common plane parallel to the substrate surface;

electrically conductive regions (75; col 7 ln 22-24) arranged in openings in each of the first and second metal lattices and electrically isolated from the intersecting metal

leads (75 isolated by dielectric from 68 & 69; Fig 3), the electrically conductive regions spaced apart from edge regions of the openings by the insulation layer and electrically isolated from one another by the intersecting metal leads,

wherein the intersecting metal leads have a width (of 69) equal to the distance between the edge regions of the openings and the electrically conductive regions; and

wherein the first and second metal lattices are laterally offset from one another, such that the electrically conductive regions of the first metal lattice (uppermost 75) are substantially vertically above crossing points of the second metal lattice (64 at 65), and crossing points of the first metal lattice (68 at 69) are substantially vertically above the electrically conductive regions of the second metal lattice (75); and

first and second electrical connections between the first and second lattices such that the first and second electrical connections are at different electrical potential (inherent in connection to different polarities: col 7 ln 21-24, col 8 ln 39-46).

Ng differs from the claimed invention in not showing electrically conductive regions in each of at least two openings in each of the metal lattices.

Ng is directed to a multi-layer capacitor for high-frequency circuits (col 1 ln 8-10).

Kuroda is analogously directed to a multi-layer capacitor for high-frequency circuits (col 1 ln 13-15) and teaches a structure having advantageously improved electrical properties (col 3 ln 25-30) stemming from the pattern of current flow within the multi-layer capacitor (col 12 ln 58-62). The particular current patterns (col 8 ln 32-34) are due to alternating and offset (col 7 ln 1-11) first (10, Fig 3A) and second (11, Fig 3B)

metal lattices which each include electrically conductive regions (17 in Fig 3A, 16 in Fig 3B, col 8 ln 3) isolated in each of at least two cutouts (18, col 7 ln 62 – col 8 ln 18).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the capacitor structure of Kuroda in the semiconductor component of Ng, essentially replacing Ng Fig 2 with Kuroda Fig 2, such that electrically conductive regions arranged in each of at least two openings in each of the metal lattices; at least for a semiconductor component having an integrated capacitance structure with advantageous electrical properties.

The combination of Ng and Kuroda arguably differs from the claimed invention only in not explicitly disclosing the intersecting metal leads having a width less than or equal to the distance between the edge regions of the openings.

Ng clearly shows the claimed width relationship, Kuroda seems to depict leads so wide that their crossing essentially defines a sheet with what is depicted as relatively small holes. However, the scope of Kuroda is in no way limited by the width of the leads or the opening size. It seems the designer may choose to adjust the width.

Baker is analogously directed to a capacitor in an integrated circuit (col 1 ln 5-8) and is evidence that the claimed relationship between conductor width (col 4 ln 50) and the distance between edges of opposite capacitor plates (col 4 ln 51-52) is known to be a variable affecting the resultant capacitance (col 4 ln 59-64).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in the combination of Ng and Kuroda, the intersecting

metal leads have a width less than or equal to the distance between an edge of the openings and the electrically conductive regions; at least for the desired capacitance.

RE claim 12, the combination includes, as Kuroda discloses (Figs 3-4) the electrically conductive regions (17 in Fig 3A, 16 in Fig 3B) of the first (10) and second (11) metal lattices comprise metal plates or node points.

RE claim 13, the combination includes, as Kuroda discloses (Figs 3-4) the electrical connections comprise:

first connecting lines (17) electrically connecting the electrically conductive regions of the first metal lattice (10) to crossing points (17) of the intersecting metal leads of second metal lattice (11, col 8 ln 4-10); and

second connecting lines (16) electrically connecting crossing points (16) of the intersecting metal leads of the first metal lattice (10) to the electrically conductive regions (16) of the second metal lattice (11, col 8 ln 4-10).

RE claim 14, the combination includes, as Kuroda discloses a metal plate (e.g., 14 or 15) in a third common plane parallel to the substrate surface and electrically coupled to the first and second metal lattices by the first and second electrical connections (col 7 ln 32-39 & 53-61).

RE claim 15, The combination includes, as Kuroda discloses (Figs 3-4) a third metal lattice (e.g., bottom 10 in Fig 4) including intersecting metal leads in a third common plane parallel to the substrate surface, wherein the intersecting metal leads define openings (18) and wherein the intersecting metal leads are electrically connected to the first and second metal lattices by the electrical connections (72, 74).

The combination differs from the claimed invention in not disclosing the third metal lattice openings devoid of electrically conductive regions.

Baker discloses an optional reference plate or layer (302, col 5 ln 41-45) which forms an additional capacitance (col 6 ln 5-9).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in the combination of Ng and Kuroda, there be a third metal lattice devoid of electrically conductive regions; at least to use a know suitable method of further increasing the capacitance.

Claims 22 and 23 are rejected under 35 U.S.C. § 103(a) as unpatentable in view of Kuroda and Ng.

RE claim 22, Kuroda discloses a capacitance component comprising (Fig 1-4):

a first metal lattice (10, Fig 3A) extending in a plane (Fig 4) and including crossing metal leads that define crossing points (16) and a plurality of openings (18, col 8 ln 13) therein, where each of the plurality of openings are circumferentially enclosed by the crossing metal leads;

first connecting lines (16) electrically connected to the first metal lattice (Fig 4, also col 7 ln 52-57);

first electrically conductive regions (17, col 7 ln 57) comprising one of metal plates or node points between via connections in the plurality of openings in the first metal lattice and electrically isolated from the crossing metal leads; and

second connecting lines (17) electrically connected to the first electrically conductive regions and electrically isolated from one another by the first metal lattice.

Kuroda differs from the claimed invention only in not disclosing the capacitance component being a semiconductor capacitance component.

Kuroda is a multi-layer capacitor for high-frequency circuits (col 1 ln 13-15).

Ng is analogously directed to a multi-layer capacitor for high-frequency circuits (col 1 ln 8-10) and discloses a semiconductor capacitance component in that the capacitance component (50, col 6 ln 52-55) is formed on the semiconductor substrate (53, col 6 ln 60) as part of an integrated circuit (col 1 ln 6-9, col 6 ln 52).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the capacitance component of Kuroda be integrated on a semiconductor substrate, giving a semiconductor capacitance component; at least for increased integration, as is the driving trend of this art.

RE claim 23, Kuroda discloses a second metal lattice (11, Fig 3B) extending in a second plane (Fig 4) and including crossing metal leads that define crossing points (17) and a plurality of openings (18) therein, where each of the plurality of openings are circumferentially bounded by the crossing metal leads; and

second electrically conductive regions (16) in the plurality of openings of the second metal lattice and substantially vertically aligned with the crossing points of the first metal lattice (Fig 4) wherein the first connecting lines electrically connect the crossing points of the first metal lattice to the second electrically conductive regions,

and the second connecting lines electrically connect the first electrically conductive regions to the crossing points of the second metal lattice (col 7 ln 62 – col 8 ln 17).

Conclusion

Hu (US 6,743,671) is cited and not relied upon but is relevant for teaching a multi-layer capacitor including a metal plate (43) for shielding.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of time extension per 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. For more info about PAIR, see http://pair-direct.uspto.gov. For questions PAIR access, contact the Electronic Business Center at 866-217-9197 (toll-free). For assistance from a USPTO Customer Service Rep or access to the automated info system, call 800-786-9199 or 571-272-1000.

/Andrew O. Arena/
Examiner, Art Unit 2811
6 May 2009

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811